Instructor

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Office Hours : zoom call by appointment

Netiquette

Carleton guidelines https://carleton.ca/online/online-learning-resources/netiquette/.

This class or portions of this class will be recorded by the instructor for educational purposes. These recordings will be shared only with students enrolled in the course. Your can access the recordings from the class online lectures section of the course webpage below.

Unauthorized student recording of classroom or other academic activities (including advising sessions or office hours) is prohibited. Unauthorized recording is unethical and may also be a violation of University policy. Students requesting the use of assistive technology as an accommodation should contact the Paul Menton Centre. Unauthorized use of classroom recordings – including distributing or posting them – is also prohibited. Under the University's Copyright Policy, faculty own the copyright to instructional materials – including those resources created specifically for the purposes of instruction, such as lectures slides, lecture notes, and presentations. Students cannot copy, reproduce, display, or distribute these materials or otherwise circulate these materials without the instructor's written permission. Students who engage in unauthorized recording, unauthorized use of a recording, or unauthorized distribution of instructional materials will be referred to the appropriate University office for follow-up.

During class, all students must enter the class zoom session using there real name and should mute there microphone unless instructed to unmute by the instructor or moderator

During class, student should post questions or comments to the zoom chat which will then be addressed by the instructor or moderator. Keep chat comments focused on course content and keep language respectful.

If students experience difficulties joining a class Zoom session or are dropped from the session a recording of the class Zoom session will be posted on the online class lectures section of the course web page

Labs will be carried out using Microsoft teams. Students should use the same netiquette guidelines for lab sessions.

Learning Objective

The objective of this course is to introduce the student to design of CMOS logic gates, digital circuit design using Verilog HDL and logic synthesis, asynchronous to synchronous interfacing,

clock distribution and timing issues, digital circuit implementation and verification, digital memory and signalling technologies.

Learning Outcomes

A student who successfully fulfills the course requirements will have demonstrated an ability to:

1. define the three levels of abstraction used in digital design
2. design digital gates using NMOS, PMOS and CMOS logic families that implement boolean functions
3. define the voltage transfer characteristics of a digital inverter
4. design MUXes, latches and flip-flops using CMOS logic
5. design linear feedback shift registers (LFSRs) that produce pseudo-random bit patterns
6. design combinational and sequential logic circuits that can be synthesized using Verilog HDL
7. define setup time, hold time and propagation delay of a flip-flop
8. define synchronous and asynchronous signals
9. define metastability and its effects on the output of a flip-flop
10. design synchronization circuitry for interfacing asynchronous signals with synchronous circuits
11. define positive and negative skew
12. design circuits that perform effectively in the presence of clock skew
13. implement digital circuits using FPGAs
14. define digital verification and testing
15. define random access memory (RAM), read only memory (ROM) and electrically erasable programable read only memory (EEPROM)
16. use computer-aided tools in a lab environment with a lab partner to design, construct, simulate and test digital circuits
17. write lab reports, answer essay type questions using text, equations and numeric values for assignments and examinations

References

Jan Rabaey, *Digital Integrated Circuits*, Prentice Hall, 1996
S. Palnitkar, *Verilog HDL*, Prentice Hall, 1996
J. P. Hayes, *Introduction to Digital Logic Design*, Addison Wesley, 1993

Marking Scheme

Laboratory	30%	**Students must complete all labs**
Assignments	10%	
Midterm Exam	15%	Thurs. March 3rd, 2022 during class
Final Exam	40%	**Students have to pass the final exam to pass course**
Bonus Quizzes	10%	

- *Please note that the final examination in this course will use a remote proctoring service provided by Scheduling and Examination Services. You can find more information at https://carleton.ca/ses/e-proctoring/.*

Teaching Assistants

		By Appointment ONLY
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Week	Dates in 2022	Lectures	Labs	Assignments/Readings/Comments
0,1	Jan 10-21	Introduction & MOSFET		
2	Jan 24-28	CMOS Logic Gates		Also some discussion on Asynchronous Circuits in preparation for labs
3	Jan 31 - Feb 4	CMOS Logic Gates and Intro to Verilog HDL		Assignment 1, due Feb. 17 , 2022
4	Feb 7-11	Verilog HDL I		Introduction to Verilog Example verilog code
5	Feb 14-18	Verilog HDL II Sequential Circuits		Assignment 2, due Mar. 3 , 2022
6	Feb 21-25	Digital Circuit Implementation		**Winter break no classes or labs**

7	Feb 28-Mar 4			**Review old midterm Mar. 1 in class Midterm on Thurs. Mar. 3 during class**
8	Mar 7-11	Digital Circuit Implementation		
9	Mar 14-18	Asynchronous		
10	Mar 21-25	System Clocking		Assignment 3, due April 7, 2022
11	Mar 28-Apr 1	Digital Design Verification		
12	Apr 4-8	Memory and Signal Technologies and Review		
13	Apr 12	Review		