Fall 2020

Digital Electronics - ELEC 3500

Learning Objective

This objective of this course is to introduce the student to design of CMOS logic gates, digital circuit design using Verilog HDL and logic synthesis, asynchronous to synchronous interfacing, clock distribution, glitches/hazards and metastability.

Learning Outcomes

A student who successfully fulfills the course requirements will have demonstrated an ability to:

1. define the three levels of abstraction used in digital design
2. design digital gates using NMOS, PMOS and CMOS logic families that implement boolean functions
3. define the voltage transfer characteristic (VTC) of a digital inverter
4. design MUXes, latches and flip-flops using CMOS logic
5. design linear feedback shift registers (LFSRs) that produce pseudo-random bit patterns
6. design combinational and sequential logic circuits that can be synthesized using Verilog HDL
7. predict the presence of glitches and hazards in sequential circuits
8. redesign circuits to remove glitches and mask hazards in sequential circuits
9. define setup-, hold-time and propagation delay of a flip-flop
10. define synchronous and asynchronous signals
11. define metastability and its effects on the output of the flip-flop
12. design synchronization circuitry for interfacing asynchronous signals with synchronous circuits
13. define positive and negative clock skew
14. design circuits that perform effectively in the presence of clock skew
15. implement digital circuits using FPGAs
16. use computer-aided tools in a lab-environment with a lab-partner to design, construct, simulate and test digital circuits
17. write lab-reports, answer essay-type questions using text, equations and numeric values for assignments and examinations

Instructor

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Evaluation Scheme

Labs	20%
Assignments	10%
Midterm	20%
Final	50%

Lab exemptions cannot be given for accreditation purposes. Students need to obtain a minimum of 50% in their term mark (labs + assignments + midterm), final examination and the total mark in order to pass the course. Students should also do all the labs and get 50% or higher in their overall lab mark to pass this course.

References

- *Course notes* and *lab notes* available on cuLearn
- J. Rabaey, *Digital Integrated Circuits*, Pearson/Prentice Hall 1996.

- S. Palnitkar, *Verilog HDL*, Prentice Hall, 1996.
- J. P. Hayes, *Introduction to Digital Logic Design*, Addison Wesley, 1993.

Miscellaneous Notes

1. Students with disabilities requiring academic accommodations in this course are encouraged to contact a coordinator at the Paul Menton Centre for Students with Disabilities to complete the necessary letters of accommodation. After registering with the PMC, make an appointment to meet and discuss your needs with the course instructor at least two weeks prior to the first in-class test or midterm exam. This is necessary in order to ensure sufficient time to make the necessary arrangements.
2. Requests for religious accommodations should be sent to the course instructor by the end of September 2020. Religious obligations that coincide with the mid-term will be dealt with by moving the weight of the mid-term to the final.