A NOVEL CMOS EDGE EQUALIZER FOR 10-GB/S HIGHLY LOSSY BACKPLANE

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ABSTRACT

This paper presents a novel CMOS edge equalizer for 10-Gb/s transceivers for backplane channels with high loss. The equalizer reduces ISI at edges and ISI at data centers simultaneously without incurring multilevel signaling. Unlike conventional edge equalizer that recovers data from current sample and previous sample, this equalizer recovers data only from current sample so that error propagation is avoided. It requires much less high-frequency boost while maintaining the amenity for CMOS implementation of conventional CMOS feed-forward-equalizer. The equalizer is implemented in TSMC 90-nm CMOS technologies. Comparison shows for highly lossy backplane applications, it is superior to decision-feed-back-equalizer, linear-feed-forward-equalizer, and conventional edge equalizer.

1. INTRODUCTION

Gigahertz-speed data transmission is required in high-capacity multi-service switches (MSSs) such as core routers and cross-connected switches [1]. As a result, the next generation MSSs will employ 10-Gb/s backplane signaling. However, current low-cost backplane materials and connectors do not provide adequate bandwidth to support this transmission rate [2]. There are several approaches being pursued by many vendors to increase backplane transmission speed. These techniques fall into basically two categories of solutions. Passive solutions upgrade these backplane materials and connectors to high-quality ones. Active solutions use signal processing to overcome the poor transmission properties of the physical channel. For numerous low-quality backplane transmission systems, the frequency-response rolloff is severe, and the use of vias-holes on thick backplanes results in nulls in the frequency range of interest. It is difficult for transceivers that use NRZ signaling and conventional equalization techniques to meet symbol-error-rate (SER) specifications. Multi-level signaling can provide good transmission performance even for long trace lengths because of its ability to compress bandwidth. However, power consumption and system complexity are issues for multi-level signaling such as 4-level pulse amplitude modulation (PAM-4). In addition, conventional equalization techniques are aimed at reducing inter-symbol interference (ISI) at data centers, which usually leads to sufficiently large ISI at edges [3].

Duobinary signaling requires much less high frequency boost than conventional linear equalization techniques. Because of this, it is sometimes regarded as a bandwidth compression technique. Duobinary signaling belongs to a set of partial response (PR) equalization techniques among which some responses have no ISI at ±(n+0.5)T, where n is a positive integer. Therefore, these responses equalize data edges. However, they leave significant amount of ISI at data centers to make sampling at these points useless. Fortunately, a strictly edge-equalized response only has ISI to edges at ±0.5T. Therefore, the amplitude at edges only has 3 levels. In practice, there is some residual ISI at edges. Even though we can use 3-level signaling to detect the amplitude at edges and retrieve data from the correlation between adjacent symbols. One disadvantage of duobinary signaling is that 3-level signaling leads to more complicated circuits than NRZ signaling. Another disadvantage is possible error propagation because 1-bit datum is retrieved from 2 or more symbols. If a symbol is an error, it can propagate until it is corrected or another error occurs. Furthermore, ternary signaling has worse noise tolerance than binary signaling for a given swing of waveform.

This paper introduces a novel edge equalization technique for 10-Gb/s highly lossy backplane. In section 2, transceiver structure and basic theories of highly lossy backplane traces are reviewed. In section 3, the edge equalization method is discussed, which followed by CMOS circuit implementation in section 4. Comparison and conclusion are made in section 5 and section 6.

2. BASIC THEORIES

Figure 1. Block diagram of a popular backplane transceiver

The block diagram of a popular high-speed backplane transceiver is shown in Fig.1. In order to counteract the distortion introduced by the channel, equalization is
introduced in the transmitter side or the receiver side or both. Backplane traces are basically transmission lines. The electromagnetic wave guided by the conductors can be expressed in equation (1).

\[ E(z) = E(0) \cdot e^{-\alpha z} e^{-j\beta z} \]  

(1)

Where \( \alpha \) and \( \beta \) are attenuation constant and propagation constant, respectively. It can be inferred from equation (1) that the attenuation quadruples if the length of a transmission line doubles. Therefore, it is very challenging to use long-trace backplane. Fig.2 shows the s21 of a 20-inch backplane, a 34-inch backplane and 56-inch backplane, respectively. The slopes are -2.7dB/GHz, -3.6dB/GHz and -7.5 dB/GHz.

![Figure 2. S21 for B20, 34inchROG, and 56inchFR4 channels](image)

For highly lossy backplane channels, for example, the 56-inch channel, it is very challenging for linear equalizers to suppress ISI at data centers to an acceptable level. On the one hand, a transmitter equalizer or pre-emphasis in fact de-emphasizes or reduces the low-frequency signal envelope level in proportion to the attenuation experienced by the high-frequency pattern in the channel. The de-emphasis process also increases the relative strength of the high-frequency content of the transmitted signal, thereby increasing the proportion of total signal power coupled into an adjacent line through a high-pass parasitic coupling path;

On the other hand, a receiver linear equalizer inevitably suffers from noise enhancement. For backplane traces with very high loss, PAM-4 is definitely superior to NRZ and duobinary signaling. However, system complexity and power consumption usually overshadow its advantages.

In applications such as magnetic storage or optical storage, another bandwidth compression method other than multi-level is extensively used. The method is called runlength limited (RLL) channel coding. In fact, RLL encoder must be implemented in the transmitter side of any backplane transceiver, because in backplane transceivers, there is not an exclusive clock signal, clock is retrieved from transition edges. Long consecutive data patterns may occur without RLL encoder and phase-locked-loop (PLL) may stray away. 8b/10b code is an RLL code that is most extensively used in backplane transceivers. It restricts the longest runlength so that the maximum digit-sum-value (DSV) is 6. However, it does not have ability to compress bandwidth, since it does not limit the shortest runlength. RLL(1,7) code that has a shortest runlength of 2 and coding efficiency of 2/3 is extensively used in storage applications [4]. Normalized to 8b/10b, its total coding efficiency is 5/6. However, the bandwidth is compressed to 60%. This technique is vaguely mentioned in [5]. In Fig.2, this technique means the bandwidth is moved from point A to point B, which has gained about 20 dB.

The advantages of RLL channel coding can not be fully explored if the equalization method is aimed to suppress ISI at data centers, because instead of decreasing the data rate, the coding actually increases it. Another technique that we apply in this paper is edge equalization.

### 3. THE PROPOSED EQUALIZER

In high-speed backplane transceivers, equalizer and CDR are closely correlated. On the one hand, equalizer suppresses ISI at data centers and edges so that CDR can work properly; On the other hand, discrete-time equalizer utilizes the clock generated by CDR to sample the incoming waveform and perform filtering. In many applications, the SER bathtub only has a small bottom. Clock jitter or clock phase offset can easily lead to unacceptably high SER. Unfortunately, conventional equalization methods are unable to suppress ISI at data centers and edges equally well, especially for highly lossy channels. Conventional edge equalizers suppress ISI at edges but leave a large amount of ISI at data centers. As a consequence, multi-level signaling at edges has to be introduced in the receiver side, which is an unwanted side effect leading to more system complexity and reduced noise tolerance for a given voltage swing. Equation (2) gives the time-domain impulse response of a popular edge equalizer.

\[ h(t) = \frac{\pi}{4} \left[ \sin \left( \frac{t}{T} + 0.5 \right) + \sin \left( \frac{t}{T} - 0.5 \right) \right] \]  

(2)

Where \( t=0 \) is the data center and \( t=(n+0.5)T \) is the edge. Equation (3) gives the frequency-domain response.

\[ |H(f)| = \frac{\pi}{4} \cdot T \cdot e^{j\pi/2} \left( 1 + e^{-j\pi/2} \right) \cdot \text{rect} \left( \frac{Tf}{f_{\text{symbol}}} \right) \approx 1 + z^{-1} \]  

(3)

Therefore, the target response of the popular edge equalizer is actually duobinary signaling. According to the hybrid analytical model described in [6], at data centers, the sampled version of the received signal \( y(t) \) can be expressed as follows.

\[ y(t_s) = \sum_{k=-\infty}^{\infty} a(k) h(t_s - kT) = \sum_{k=-\infty}^{\infty} a(n-k) h(kT) \]  

(4)

\[ h(kT) = \cos \left( \frac{k\pi}{4} \right) \]  

(5)

Equation (4) can be recast into equation (6).

\[ y(t_s) = a(n) + \sum_{k=0}^{\infty} a(n-k) \frac{\cos \left( \frac{k\pi}{4} \right)}{1 - 4k^2} \]  

(6)
The worst cases of destructive ISI are when \( a(n) = 1 \), every item in the second part of equation (6) is negative, and when \( a(n) = -1 \), every item in the second part of equation (6) is positive. The total ISI can be calculated to be 1.

Therefore, the vertical eye opening is completely eroded by ISI. In practice, the worst case will never happen because of the implementation of RLL channel code such as 8b/10b. However, the vertical eye opening becomes so small that we are reduced to use 3-level signaling at edges and to retrieve data from the correlation of adjacent symbols. Allowing the shortest runlength to be 1 baud period is the root cause leading to 3-level signaling and the system complexity. If advanced channel code such as RLL(1,7) code is applied, the worst cases will be much better than the worst cases mentioned above. The reason is that since the shortest runlength is 2 baud periods, 101 (or 1, -1, 1) and 010 (or -1, 1, -1) will never happen. There is always constructive ISI comes from one of its two neighbors. This ISI doubles its effect, because it is assumed to be destructive. The maximum amplitude of ISI is now reduced to 1/3. Therefore, the vertical eye is open, because the data is 3 times the value of the maximum ISI. In addition, the horizontal eye is also open, because the target response is edge equalization.

4. CMOS IMPLEMENTATION

\[ \begin{align*}
\text{Figure 3.} & \quad 5\text{-tap FIR pre-emphasis} \\
\end{align*} \]

Seen from the above discussion, the proposed edge equalizer can be implemented in a similar way as conventional FFE. The channel encoder and decoder are realized in parallelism. One can even realize it in software. The equalizer can be implemented in the transmitter side or the receiver side. In this paper, it is implemented in the transmitter side as shown in fig. 3. It basically is 5-tap programmable FIR pre-emphasis. Registers and single-to-differential (S2D) circuits are implemented in rail-to-rail CMOS circuits. All other circuits are implemented in CML. Each tap consists of DFFs for retiming, XORs for coefficient sign control, buffers, 5-bit programmable current source (iDAC) to control the weight of each tap, and 6-bit registers to store the optimized coefficients. The sign of the coefficients is the most significant bit (MSB).

The equalizer is implemented in TSMC 90-nm CMOS technology using power supply of 1.2V. Simulation shows the power consumption for 10-Gb/s is 65 mW.

5. THE SIMULATION RESULTS

The proposed edge equalizer can open the eye of the highly lossy 56-inch backplane with 5-tap pre-emphasis. The eye diagram is shown in fig.6. The eye opening is about 1/3 of the peak-to-peak value of the received waveform, which verifies our analysis in section 3. In fact, the eye opening is a bit better than 1/3; because RLL channel coding actually contributes more than one symbol constructive ISI. The eye diagram can be reshaped by using a limiting amplifier.

\[ \begin{align*}
\text{Figure 4.} & \quad \text{(a) D-latch (b) XOR (c) buffer} \\
\text{Figure 5.} & \quad \text{5-bit programmable current source} \\
\text{Figure 6.} & \quad \text{Equalized eyediagram of a 5-tap equalizer (this paper)} \\
\end{align*} \]
As comparison, the simulated eye diagram of the simulated eye diagram of a 10-tap conventional edge equalizer, the simulated eye diagram of a 10-tap zero-forcing (ZF) pre-emphasis, and the simulated eye diagram of a 10-tap conventional DFE (without a FFE) are shown in fig.7, fig.8, and fig.9, respectively. It is clear that those equalization methods can not open the eye at data centers even if 10-taps are used. Although the ZF pre-emphasis has a very small eye opening at data centers, in reality, the excessive high frequency boost and noise enhancement will eventually close the eye. Therefore, this equalizer is superior to those structures in terms of number of taps, power consumption and system simplicity. However, limited by the power supply voltage swing in the transmitter side, this equalizer has a smaller peak-to-peak voltage than DFE. For this reason, it might be advantageous to implement this equalizer in the receiver side. However, it requires much more efforts in circuit design.

6. CONCLUSION

A novel edge equalizer is proposed. By applying advanced techniques such as bandwidth compression, edge equalization, and constructive ISI, the equalizer can open the eye diagram of a highly lossy 56-inch backplane with 5-tap FIR pre-emphasis. It reduces ISI at edges and ISI at data centers simultaneously without using multilevel signaling techniques. It also can recover data only from current sample. This equalizer is superior to decision-feed-back-equalizer, linear-feed-forward-equalizer and conventional edge equalizer in terms of number of taps and system simplicity.

REFERENCES