SoC With an Integrated DSP and a 2.4-GHz RF Transmitter

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Abstract—We present a system-on-chip (SoC) that integrates a TMS320C54x digital signal processor (DSP), which is commonly used in cellular phones, with a multigigahertz digital RF transmitter that meets the Bluetooth specifications. The RF transmitter is tightly coupled with the DSP and is directly mapped to its address space. The transmitter architecture is based on an all-digital phase-locked loop (ADPLL), which is built from the ground up using digital techniques and digital creation flow that exploit high speed and high density of a deep-submicrometer CMOS process while avoiding its weaker handling of voltage. The frequency synthesizer features a wideband frequency modulation capability. As part of the digital flow, the digitally controlled oscillator (DCO) and a class-E power-amplifier are created as ASIC cells with digital I/Os. All digital blocks, including the 2.4-GHz logic, are synthesized from VHDL and auto routed. The use of VHDL allows for a tight and seamless integration of RF with the DSP. To take advantage of the direct DSP-RF coupling and to demonstrate a software-defined radio (SDR) capability, a DSP program is written to perform modulation of the GSM standard. The chip is fabricated in a baseline 130-nm CMOS process with no analog extensions and features high logic gate density of 150 kgates per mm². The RF transmitter area occupies only 0.54 mm², and the current consumption (including the companion DSP) is 49 mA at 1.5-V supply and 4 mW of RF output. This proves attractiveness and competitiveness of the “digital RF” approach, whose goal is to replace RF functions with high-speed digital logic gates.

Index Terms—All-digital, Bluetooth, digital signal processor (DSP), frequency synthesizer, integration, phase domain, single-chip, system-on-chip (SoC), transmitter.

I. INTRODUCTION

With the explosive growth of the wireless communications industry worldwide, the need has arisen to reduce cost and power consumption of mobile stations. The use of deep-submicrometer CMOS processes allows for an unprecedented degree of scaling and integration in digital circuitry, but complicates the implementation of traditional RF and analog circuits. Consequently, a needed has arisen to find digital architectural solutions to the RF functions.

The frequency synthesizer is a key block used for frequency translation of radio signals and has been traditionally based on a charge-pump phase-locked loop (PLL), which is not easily amenable to integration. Recently, a digitally-controlled oscillator (DCO), which deliberately avoids any analog tuning controls, was first presented in [1] for RF wireless applications. This allows for its loop control circuitry to be implemented in a fully digital manner as first proposed in [2]. The references [1] and [2] only describe the DCO and its immediate digital logic in an ADPLL-based frequency synthesizer and I/Q upconverter-based transmitter. This paper presents implementation details and design flow of the IC chip.

The RF frequency synthesizer and transmitter employ a novel fully digital architecture that takes advantage of the deep-submicrometer process strengths: \( f_T \) of 100 GHz, inverter delays \( \leq 40 \) ps, low voltage of 1.5 V, and excellent control of transition edges. It achieves RF frequency synthesis using an all-digital PLL (ADPLL) architecture as per PLL classification in Best’s work [3]. This is in contrast to the conventional charge-pump-based frequency synthesizer and I/Q upconverter-based transmitter architectures that rely on large-voltage analog-intensive circuits. Due to its programmability, flexibility, and portability, the digital RF transmitter serves as a foundation of a digital radio processor (DRP). The challenge of the above ADPLL-based transmitter is to find an architecture that is amenable to low current consumption such that it is competitive to similar products using the conventional RF techniques.

The organization of this paper is as follows. Section II presents the DSP and its interface to the digital RF transmitter. The overall transmitter architecture is shown in Section III. A low-power architecture of the 2.4-GHz counter and a sampler that operates at a lower 13-MHz comparison frequency of the phase detection is presented in Section IV, whereas Section V shows a time-to-digital converter (TDC). Section VI presents...
a high-speed flip-flop with excellent metastability resolution characteristics, which is used in the above circuits. Modeling and simulation are described in Section VII. The implementation and measured results are covered in Sections VIII and IX.

II. DSP AND ITS RF INTERFACE TO DRP

Overview of the IC chip is presented in Fig. 1. The Texas Instruments TMS320C54x DSP is equipped with 28 kwords of RAM and 128 kwords of ROM and contains typical peripherals used for cellular applications: timer, API, serial port, and the XIO parallel bus interface including interrupts and wait states. The XIO bus is a dedicated high-speed bi-directional parallel interface of 8-b address space and 16-b data registers that directly couple the digital RF transmitter (DRP) to the DSP. The transmitter registers are mapped into the DSP XIO space and can be accessed using read and write instructions. The DRP is the sole provider of the DSP clock. In order to avoid injection pulling of the DCO to the \( n \)th harmonic of the reference frequency, the DSP either runs on the retimed FREF clock by the DCO edge or the down-divided DCO clock. A watchdog timer automatically switches to the FREF clock if the selected clock failure is detected.

III. DIGITAL RF TRANSMITTER

The transmitter (Fig. 2) is based on an ADPLL with a wideband frequency modulation capability. The output \( \text{variable frequency} (f_V) \) is related to the \( \text{reference frequency} (f_R) \) by the frequency command word (FCW)

\[
FCW[k] = \frac{f_V[k]}{f_R},
\]

The FCW is time-variant and is allowed to change with every cycle \( T_R = 1/f_R \) of the frequency reference (FREF) clock. The ADPLL operates in the phase domain as follows [5]. The variable phase \( R_V[k] \) is determined by counting the number of rising clock transitions of the DCO oscillator clock CKV

\[
R_V[i] = \sum_{i=0}^{k} 1.
\]

The index \( i \) indicates the DCO edge activity. The reference phase \( R_R[k] \) is obtained by accumulating FCW with every cycle of the retimed frequency reference (FREF) clock input operating at \( f_R \)

\[
R_R[k] = \sum_{i=0}^{k} FCW[i].
\]

The FREF-sampled variable phase \( R_V[k] \) is subtracted from the reference phase \( R_R[k] \) in a synchronous arithmetic phase detector producing phase error samples \( \phi_E[k] \)

\[
\phi_E[k] = R_R[k] - R_V[k] + \epsilon[k].
\]

The FREF retiming quantization error \( \epsilon[k] \) is determined by the time-to-digital converter (TDC). The TDC is built as a simple array of inverter-delay elements and flip-flops, which produces a time-conversion resolution finer than 40 ps in this 130-nm process.

The phase operation of \( R_R[k] \) and \( R_V[k] \) could be visualized as two rotating vectors and the smaller angle between them constituting the phase error, as shown in Fig. 3. Both \( R_R[k] \) and \( R_V[k] \) are positive numbers, and their maximum value possible without rollover depends on the counter width or integer part of the FCW and equals \( 2^8 \). The phase error has the same range but is symmetric around zero, i.e., it is a 2’s complement number.

The digital phase error \( \phi_E[k] \) is attenuated by the loop gain factor \( \alpha \) and then normalized by the DCO gain \( K_{DCO} \) in order to correct the DCO phase/frequency in a negative feedback manner with the loop dynamics that are independent from variations in the manufacturing process, in the supply voltage, and in the
0, 2π(mod-2^{15})

Fig. 3. Rotating vector interpretation of the reference and variable phases.

TABLE I
ADPLL PHASE-DOMAIN SIGNALS

<table>
<thead>
<tr>
<th>math notation</th>
<th>name</th>
<th>bus width</th>
</tr>
</thead>
<tbody>
<tr>
<td>FCW</td>
<td>frequency command word</td>
<td>W_I + W_F</td>
</tr>
<tr>
<td>R_V[k]</td>
<td>reference phase</td>
<td>W_I + W_F</td>
</tr>
<tr>
<td>R_V[k]</td>
<td>variable phase</td>
<td>W_I</td>
</tr>
<tr>
<td>f_e[k]</td>
<td>sampled variable phase</td>
<td>W_I</td>
</tr>
<tr>
<td>f_e[k]</td>
<td>fractional error correction</td>
<td>W_F</td>
</tr>
<tr>
<td>f_e[k]</td>
<td>phase error</td>
<td>W_I + W_F</td>
</tr>
</tbody>
</table>

operating temperature [4]. The phase error attenuator factor α establishes the PLL loop first-order filtering characteristic [5]

\[ f_{BW} = \frac{\alpha \cdot f_R}{2\pi} \]  

(5)

where \( f_{BW} \) is a 3-dB cut-off frequency of the closed PLL loop. The α value is programmable with the default of \( \alpha = 2^{-8} \), resulting in \( f_{BW} = 8 \text{ kHz} \), which was chosen to be the best tradeoff between the phase noise of the reference input and the DCO phase noise.

With \( W_F = 15 \) fractional part wordlength of the fixed point \( R_R[k] \) accumulator, the ADPLL provides fine frequency control with 400-Hz accuracy, according to

\[ \Delta f = \frac{f_R}{2W_F}. \]  

(6)

The number of integer bits \( W_I = 8 \) was chosen to fully cover the Bluetooth frequency range of \( f_V = 2400-2480 \text{ MHz} \) with the \( f_R = 13 \text{ MHz} \) reference frequency.

Table I summarizes the phase-domain signals. For the implemented architecture, \( W_I = 8 \) and \( W_F = 15 \). Implementation of the most critical digital circuits, the variable phase accumulator, and the TDC are discussed in Section IV.

Three varactor banks (process/voltage/temperature, acquisition, and tracking) are sequentially activated during the frequency locking [1]. The first two banks are used for the DCO center frequency calibration, and channel selection with the step size of 2.3 MHz and 460 kHz, respectively, and use wide-loop bandwidth to provide fast loop dynamics. The tracking bank is used during the actual transmission and has the finest frequency step size of 23 kHz. The fine frequency resolution is obtained through high-speed ΣΔ dithering of the varactors.

In the feedforward path of the DCO, the CKV clock toggles an NMOS transistor switch constituting a class-E digitally controlled power amplifier (PA), as shown in Fig. 4. The matching network filters the second and higher harmonics of the carrier and is tuned to provide 4 dBm of output RF power.

IV. VARIABLE PHASE ACCUMULATOR

As shown in Fig. 5, the variable phase accumulator is implemented as an incrementer of \( R_V[k] \) followed by a sampler of \( R_V[k] \). The 8-b accumulator implements the DCO clock count incrementing with a rollover effect, which is naturally handled with the modulo (nonsaturating) arithmetic.

The CMOS process is fast enough to perform the 8-b binary incrementer at 2.4-GHz clock in one cycle using a simple carry-ripple structure. Critical timing of this operation would comprise a chain of seven half-adders and an inverter. However, for a commercial application, it was necessary to add an extra timing margin in order to guarantee robust operation with acceptable yield for all of the process and environmental conditions, as well as anticipated clock distribution skew statistics. This extra margin was obtained by increasing the maximum operational speed through topological means. The carry-ripple binary incrementer was transformed into two separate smaller incrementers, as shown in Fig. 6. The first incrementer operates on the two lower order bits and triggers the higher order increment whenever its count reaches “11.” The second incrementer operates on the same CKV clock, but the 6-b increment operation is allowed now to take four clock cycles. The long critical path of the 8-b carry-ripple incrementer has thus been split and pipelined into smaller parts, allowing for the necessary timing margin.

It was discovered quite early in the design cycle that the critical path of the above partitioning was actually the increment trigger path from the lower order registers, through the NAND gate and through the six single-bit multiplex select lines and terminating on the higher order registers. The fanout of six was taking a disproportional toll on the delay, so a slight modification was done by retiming that control path. Final implementation version of the PV block is shown in Fig. 7. The triggering state is now one count earlier at “10.” The chief improvement of
INC is now capable of controls how much attenuation the MHz, and MHz, the to be used as a fractional error. The resulting, the frequency quantization is now only ps, estimation quantization \[5\] of this solution is that the register output Q is now capable of driving six multiplex select lines.

V. TIME-TO-DIGITAL CONVERTER

This solution is that the register output Q_INC is now capable of driving six multiplex select lines.

Fig. 6 shows a TDC operating on the FREF clock of 13 MHz. It measures the fractional delay difference between the FREF clock and the next rising edge of the DCO clock, CKV, with resolution of one inverter delay \(\Delta t_{\text{res}}\), which is better than 40 ps in this CMOS process. The TDC operates by passing the complementary DCO clock through the string of inverters. On each rising edge of FREF, the delayed clock vector is sampled using an array of registers whose outputs form a pseudo-thermometer code. The outputs are then converted to binary code and normalized by the DCO clock period \(T_V\) to be used as a fractional error correction \(\epsilon\). The finite TDC resolution results in a frequency estimation quantization \[5\] of

\[
\Delta f_{\text{TDC}} = f_R \cdot \frac{\Delta t_{\text{res}}}{T_V},
\]

(7)

With \(\Delta t_{\text{res}} = 40\) ps, \(f_V = 2100\) MHz, and \(f_R = 13\) MHz, the TDC frequency estimate quantization level is 1.2 MHz. Obviously, this is unacceptably high for our application, so an advantage is taken here of the fact that the frequency is a time derivative of phase and the frequency resolution could be enhanced with a longer observation interval, i.e., over multiple FREF cycles. The scaling factor \(\alpha\) controls how much attenuation the phase error must undergo before affecting the DCO frequency. In the frequency domain, it controls a fraction of the frequency detected in response to the frequency changed at the DCO input. For a stable system, \(\alpha\) must be less than unity. The resulting ADPLL frequency quantization is governed by the following formula:

\[
\Delta f_{\text{res}} = \alpha \cdot f_R \cdot \frac{\Delta t_{\text{res}}}{T_V}.
\]

(8)

For \(\alpha = 2^{-8}\), the frequency quantization is now only \(\Delta f_{\text{res}} = 4.9\) kHz, which is sufficient for a Bluetooth transmitter.

To achieve good TDC linearity, the flip-flops must have symmetrical resolution characteristics. This requirement is here satisfied by a symmetrical flip-flop topology described below.

VI. SENSE-AMPLIFIER-BASED FLIP-FLOP

Fig. 9 shows a schematic of the high-speed tactical sense-amplifier-based flip-flop adapted from [6] that is used in the variable phase accumulator and TDC. It has been successfully used in high-speed designs in prior CMOS process technology nodes, such as in [7]. The variable counter operates at high speed but requires the coarse resolution that is typical of a digital signal, which is satisfied when the setup and hold times of the flip-flops are met. The TDC operates at a lower 13-MHz clock but requires precise timing resolution much better than the inverter delay. Consequently, both requirements are satisfied with a high-speed tactical flip-flop, which has symmetrical resolution characteristic of positive and negative data transitions. The flip-flop topology was compared against other flip-flop architectures for the similar current consumption and was found to be the fastest.

The tactical flip-flop consists of two blocks: a pulse generator SA (top of the figure) and a symmetric slave set–reset (SR) latch (bottom of the figure). It is different from the conventional master–slave latch combination in that the pulse generator is not level sensitive but generates a pulse of sufficient duration on either Sb or Rb outputs as a result of changes in clock and data values. The SR latch captures the transition and holds the state until the next rising edge of the clock. After the clock returns to
its inactive state, both Sb and Rb outputs of the SA stage assume logic high value.

Metastability is a physical phenomenon that limits performance of comparators and digital sampling elements, such as latches and flip-flops. It recognizes that it takes a nonzero amount of time from starting of the sampling event in order to determine the input level or state [9]. This resolution time gets exponentially larger if the input state change gets close to the sampling event. In the limit, if the input changes at exactly the same time as the sampling event, then it might theoretically take an infinite amount of time to resolve. During this time, the output can dwell in an illegal digital state, somewhere between 0 and 1. Fig. 10 shows a clock-to-output (CLK-to-Q) delay versus input-to-clock (D-to-CLK) skew of a high-performance flip-flop from the GS40 [8] digital standard-cell library distributed for the utilized 130-nm process. It reveals that the fall and rise transitions are not symmetric and the uncertainty zone differs in location by as much as 65 ps between the edges. This is clearly not acceptable if the required resolution would be below 65 ps. Fig. 11 shows the same plot for the tactical flip-flop developed specifically for the 2.4 GHz digital operations. It enjoys low CLK-to-Q delay, negative setup time, an extremely small metastability window and symmetric response for rise and fall data transitions, which is important for the TDC operation. For example, within a resolution time of one cycle of the RF Bluetooth period, 417 ps, the resolution window is only a few picoseconds. For the variable phase accumulator operation and the sampler, the symmetric property is not critical. However, the flip-flop figure-of-merit of CLK-to-Q delay plus the setup time is only about 100 ps.

VII. VHDL MODELING AND SIMULATION

The RF circuit behavior is modeled in VHDL using real-valued signals. The rest of the RF transmitter is synthesizable from a register transfer level (RTL) subset of VHDL, auto-placed and auto-routed. A portion of the digital logic operates at the 2.4-GHz clock frequency. The use of VHDL allows for a tight and seamless integration of RF with the DSP. Simulation of the entire transmitter, including the DSP, is carried out to determine the RF performance at the communication packet level. DCO modeling in VHDL is described in [10].

The circuits are modeled at various abstraction levels, as shown in Table II. As an example, level-1 representation of an GFSK transmit filter might describe the behavior with a simple direct-form finite-impulse response (FIR) filter equation using real numbers for input, output, coefficients, and all of the intermediate signals. Level-2 representation of the actual implementation with accumulated coefficients might show the top-level structure of major building blocks, which are then modeled behaviorally on the bit level using integers. Second-order effects, such as LSB truncation and rounding as
Fig. 11. CLK-to-Q delay as a function of data-clock timing skew relationship—tactical flip-flop (“Bora”). The data can change after the clock edge, hence the negative setup time.

TABLE II
VHDL MODELING ABSTRACTION LEVELS

| Level-1 | Mathematical equations and high-level behavioral description. Parameterized for easy analytic “what-if” questions. Optimized for simulation speed and flexibility. Fast enough to replace MATLAB for a bit error rate analysis. Includes important hardware-related nonidealities and second order effects. |
| Level-2 | Mathematical equations in integer domain. Implies the underlying architectural structure. If 100% pin compatible with Level-3, then it can be used for top-level connectivity verification. |
| Level-3 | Synthesizable register transfer level (RTL). |
| Level-4 | Gate-level netlist produced by a synthesis tool. It could also be the actual gate-level netlist extracted from an auto-place and route tool (APR). Accompanied by the cell and wire timing information (Vital or SDF). |

well as MSB clipping, are included. Level-3 RTL representation drives the synthesis of gate connectivity. Each higher level of modeling is expected to improve the simulation time by an order of magnitude.

The unified approach ensures interoperability of various abstraction levels within a single simulation environment. This allows simulating a system with a mixture of synthesized blocks and those that are still at the mathematical description levels.

A. Modeling of Metastability in Flip-Flops

Conventional synchronous digital design conveniently deals with metastability by specifying and meeting setup and hold time of the sequential components, such as flip-flops and latches. A major inconvenience of the ADPLL architecture is a necessity to deal with metastability as a normal occurrence expected in the course of device operation. This architecture, like any other system with mutually asynchronous clocks, requires a fair amount of attention to avoid synchronization failures, which are said to occur if the system attempts to use a signal while it is in a metastable state. A common method to deal with synchronization failures is to sufficiently increase mean time between failures (MTBF) by cascading synchronizers such that occasional errors are no longer considered a problem. However, unlike in conventional systems incorporating synchronizers in which the sufficient solution is to resolve metastability, this architecture further requires the metastability to be stochastically avoided.

The following list summarizes two ADPLL areas requiring special attention to metastability in the design, modeling and simulation phases.

1) Sampling of the delayed replica of the DCO clock by the frequency reference in the TDC requires metastability resolution.

2) The frequency reference retiming by the DCO clock requires metastability avoidance.

Attempts have been made to model the metastable behavior of flip-flops and latches in a hardware description language, such as VHDL. In [11], an exponential model of metastable behavior is described and implemented for a fundamental element of an SR latch. Unfortunately, the model is quite complex, thus degrading the simulation performance. In this research, we have chosen a much simpler but effective method to model metastability.

The metastability is modeled in the critical flip-flops by continuously inspecting the timing relationship between the data input (D) and clock (CLK) pins and producing an unknown output “X” on the data output (Q) pin if the D-to-CLK skew falls within the forbidden metastable window. Referring to Fig. 11, the metastable window is defined as an x-axis region (D-to-CLK timing skew) such that the CLK-to-Q delay on the y axis is longer by a certain amount than the nominal CLK-to-Q delay. For example, if the nominal CLK-to-Q delay is 100 ps when the D-to-CLK timing is far from critical, then the metastability window would be 20 ps if one can tolerate CLK-to-Q delay increase by 90 ps. If one can tolerate a higher CLK-to-Q increase of 170 ps, then the metastable window would drop by half to 10 ps. A question could be asked of how far this window can extend. The limitation lies in the fact that, for a tight D-to-CLK skew, the noise or other statistical uncertainty, such as jitter, could arbitrarily resolve the output in a way as to miss the input data. Therefore, for the conventional definition of the setup time, not only does output have to be free from any metastable condition, but also the input data has to be correctly captured. For this reason, the setup and hold times are conservatively defined in standard-cell libraries for the output delay increase of 10%–20% over nominal. The specific nature of the TDC vector capturing does not require this restrictive constraint. Here, any output-level resolution is satisfactory for the proper operation, as long as it is not metastable at the time of capture and, consequently, the metastable window could be made arbitrarily small.
In fact, in the implemented design, this timing window is made narrower than 1 fs.

The timing diagram of a flip-flop is redrawn in Fig. 12 to further expound on the idea. The $x$ axis denotes the periodic D-to-CLK relationship with the repetition period equal to the CLK clock period of $T_0$. The $y$ axis denotes the CLK-to-Q delay, which nominally equals $t_{CLK-Q(\text{nom})}$, but exponentially increases as data transitions closer to the capturing clock. Here, for simplicity, it is shown that the exact metastable point, where the flip-flop delay becomes very large, corresponds to the perfect alignment of the clock and data. In practical circuits, this need not be the case and, as Fig. 11 of the tactical flip-flop reveals, the metastable point is skewed by 47 ps with the data lagging the clock. This particular condition is subject to the specific circuit implementation. Just to demonstrate this point, the standard high-performance flip-flop in Fig. 10 shows that the metastable window lies on the opposite side, where the data leads the clock. This plot actually reveals two metastable windows, separated by about 65 ps, due to the asymmetry between rise and fall transitions of the conventional master–slave fully static CMOS topology. This single aspect of the traditional flip-flop makes it unsuitable for the TDC implementation which requires resolution in the range of 20–40 ps while maintaining a good linearity. Consequently, a symmetric sense-amplifier-based flip-flop appears to be a better choice.

The setup and hold violation windows ($t_{su}$ and $t_{sh}$, respectively) are centered around the clock and are defined for the D-to-CLK conditions, such that $t_{CLK-Q(\text{max})} > t_{CLK-Q(\text{max})}$, where $t_{CLK-Q(\text{max})}$ is a maximum allowed flip-flop output delay.

The timing periodicity shown in Fig. 12 is a general case where the clock multiplicity factor, i.e., the distance in number of edges between the launching and capturing clocks, could be greater than one. Generally, any timing relationship is valid as long as the D-to-CLK skew does not fall into the forbidden regions.

In our system, an advantage is taken of the fact that VHDL already supports a nine-valued digital bit type std_logic, which is an IEEE standard, and one of its levels is “X,” defined as “forcing unknown.” Referring to Fig. 8, the TDC flip-flops are modeled such that an “X” is generated on a Q output to indicate metastable region of its D-to-CLK timing. The “X” could then be detected in the pseudothermometer-code edge detector and replaced with a randomly picked “0” or “1.” It is the nature of this circuit that the metastable condition will be resolved within one full FREF clock cycle. However, due to noise, the resolution outcome is not known at the time of sampling. Therefore, a statistically probable binary result appears to be a good modeling choice for this phenomenon. For example, if the Q vector is “001110000…,” then there is a 50% chance of resolving it to either “001110000…” or “00111010000…” with the respective decoded TDC outcome of 5 or 6. The measurement error is thus contained to a single LSB.

B. Simulation Results

Fig. 13 shows the composite trajectory plot of the instantaneous frequency deviation while illustrating operation of various DCO modes. The $x$ axis is the time evolution in DCO clock units (about 417 ps). The $y$ axis is the frequency deviation from an initial value of 2402 MHz (channel 0) expressed in femtosecond time units, where $\Delta f = 5.77$ kHz.

The initial starting point is the channel frequency set to channel zero. At power-up, a “cold start” to channel four 4 MHz away is initiated. The ADPLL operates in the PVT mode by enabling the PVT oscillator controller. This controller makes very coarse (2.3 MHz) adjustments to the frequency. Next, the output of the PVT controller is put on hold and the acquisition oscillator controller is enabled. The acquisition controller quickly brings the frequency near the selected channel in
461-kHz steps. After the acquisition of the selected channel is complete, the output of the controller is put on hold and the integer and fractional tracking oscillator controller are enabled. The finest selection of the requested channel can only be accomplished using the tracking bank varactors with all of the resolution enhancement techniques possible for this capacitor bank [2]. The dynamic range of this mode has to cover the frequency resolution grid of the preceding acquisition mode. In the fast tracking mode, the frequency steps are the finest (less than 1 kHz), but the loop bandwidth could be as fast as in the acquisition mode. The tracking mode featuring the narrow loop bandwidth completes the channel acquisition and frequency locking. The locking process takes altogether 15 μs with the reference frequency of 13 MHz (about 36 thousand DCO cycles or 196 FREF cycles). Upon reaching the steady state of the acquisition, the GFSK data modulation takes place.

VIII. IMPLEMENTATION

The design is executed based on the Texas Instruments ASIC digital flow with special adjustments due to analog/RF content. The transmitter core is partitioned into the following blocks.

- **Low-speed digital** (LSD) superblock with clocks running on the retimed reference frequency of 13 MHz.
- **High-speed digital** (HSD) subchip with clocks much faster than the reference frequency; it contains variable phase accumulator (running at 2.4 GHz) and ΣΔ dithering of the oscillator tracking bank varactors (running at 600 MHz).
- **TDC ASIC cell**: the TDC operates at FREF, but it has high timing precision requirements; the ASIC cell also contains the FREF clock retiming circuit, which mostly operates at 2.4 GHz.
- **DCO+PA ASIC cell with only digital I/Os**: digitally controlled oscillator and class-E PA are conveniently combined as a single RF module. The PA consists of a digital switch transistor with the matching network built from parasitic components and components external to the IC chip; the RF devices are built using the existing devices available to DSP designers. The planar inductor is constructed using metal layers 3–5. The varactors use PPOLY/NWELL MOS structures with a fully digital control of the oscillating frequency [1].
- **Control bus interface superblock** allows the transmitter to be controlled through the XIO parallel-port interface.

Fig. 14 is a die microphotograph of the presented IC chip. It is fabricated in a baseline 130-nm CMOS process with no analog extensions and it features high digital logic density of 150 k gates per mm². It only requires a small number of external glue components. The total silicon dimensions are 3290 μm × 3290 μm, which includes 160 μm dedicated on each side for I/O pads. The companion TMS320C54x DSP, which includes typical peripherals used in 2G cellular phones, occupies 6 mm² (2430 μm × 2470 μm). The RF transmitter is located in the lower left-hand-side corner and occupies only 0.54 mm², which is the smallest ever reported. The LC-tank inductor occupies a 270 μm × 270 μm square and is clearly discernible as the biggest single component on the entire chip. This photograph dramatically illustrates the high cost, in terms of digital logic, of conventional RF components in high-density

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Supply</th>
<th>Current</th>
<th>Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low-speed digital + DSP</td>
<td>VDD</td>
<td>12.7 mA</td>
<td></td>
</tr>
<tr>
<td>High-speed digital</td>
<td>VDD-HS</td>
<td>12.8 mA</td>
<td></td>
</tr>
<tr>
<td>Oscillator</td>
<td>VDD-OSC</td>
<td>2.8 mA</td>
<td></td>
</tr>
<tr>
<td>RF w/o the oscillator</td>
<td>VDD-RF</td>
<td>21.2 mA</td>
<td></td>
</tr>
<tr>
<td>Total</td>
<td></td>
<td>49.5 mA</td>
<td></td>
</tr>
</tbody>
</table>

TABLE IV

CURRENT CONSUMPTION AT 1.5-V SUPPLY
modern CMOS processes and illustrates the benefits of digital implementation of RF synthesizers. This further provides incentives to minimize the number of classical RF components and to research novel digitally intensive architectures of RF functions.

Fig. 15 is a photograph of the evaluation board with the IC chip located at the center. The 2.4-GHz RF output, the 13-MHz frequency reference (FREF) input, and its retimed output are connected to the three SMA connectors. The connectors on the right-hand side attach the evaluation board to a PC interface board (not shown), whose purpose is to control the IC chip by means of a graphic–user interface (GUI) computer program or through a Code Composer.

IX. MEASUREMENT RESULTS

A. Performance Summary

The digital RF transmitter meets the Bluetooth specifications for RF performance. The phase noise and other performance measurements of the DCO were presented in [1]. The measured oscillator jitter at the RF port is only 100 fs, which is over an order of magnitude better than in conventional PLLs for clock generation in DSPs and microprocessors.

Table III summarizes the key measured transmitter performance parameters. The total current consumption is 49.5 mA, as shown in Table IV. It also includes the DSP under light-to-moderate loading.

B. Bluetooth GFSK Modulation

Eye diagram of the RF output with the PN9 pseudorandom modulated data is shown in Fig. 16. The observation was performed with the Rohde&Schwarz FSIQ-7 signal analyzer, which demodulates the RF signal into baseband and plots the detected instantaneous frequency deviation on the y axis. The peak-to-peak frequency deviation was measured to be 320.52 kHz, which is very close to the theoretical value of 320 kHz, calculated as the modulation index of 0.32 times the 1-Mb/s data rate frequency. It also demonstrates a very wide eye opening ratio of 86%–87% (the Bluetooth spec is ≥80%), which is desired for error-free symbol detection and very narrow zero crossings, which are desired for symbol timing and synchronization.

C. Synthesizer Switching Transients

Fig. 17 gives insight into the time-domain operation of the ADPLL. A simple DSP program was written to step the ADPLL.
through the three operational modes while observing the actual frequency deviation at the RF output. The $\times$-axis scale is 300 kHz per grid. The $\checkmark$-axis on the plot is a time progression in units of 1-$\mu$s symbols, with the scale of 20 $\mu$s per grid. The initial frequency deviation was 2 MHz. The following is the predetermined timing sequence: 1) PVT mode was operational for 5 $\mu$s; 2) the acquisition mode was then operational for 25 $\mu$s; (3) the fast tracking mode was then operational for 18 $\mu$s; and 4) the regular tracking mode was finally turned on for the remaining time. The plot shows that in the above configuration the settling time is less than 50 $\mu$s. Even though the measured value is higher than 15 $\mu$s shown in Fig. 13, it is still several times better than those reported for conventional RF PLLs. The reason for the longer settling time was found to be due to the extra unfiltered noise on the power supply lines.

D. DSP-Driven Modulation

As a demonstration of the tight operational integration between the DSP and the digital RF, a program was written to perform a software GSM modulation of the transmitter instead of using a dedicated hardware for the Bluetooth modulation.

Impulse response $h[k]$ of the Gaussian filter in the discrete-time domain is expressed as

$$h[k] = \frac{\sqrt{2\pi}}{\sqrt{\ln(2)}} \frac{BT_s}{T_s} \exp \left[ -\left( \frac{\sqrt{2\pi}}{\sqrt{\ln(2)}} \cdot \frac{BT_s \cdot k}{\text{OSR}} \right)^2 \right]$$

where $B$ is the 3-dB bandwidth, $T_s$ is the symbol period, and OSR = $f_R/(1/T_s)$ is the symbol oversampling ratio by the reference clock. For Bluetooth, $BT_s = 0.5$ and $T_s = 1 \mu$s. For GSM, $BT_s = 0.3$ and $T_s = 3.692 \mu$s. The peak RF frequency deviation is $\pm 160$ kHz in Bluetooth and $\pm 67.71$ kHz in GSM.

The GSM symbol rate is 270.833 kb/s. At the reference frequency of 13 MHz, the symbol oversampling ratio is exactly 48 (13 MHz/270.833 kHz), meaning there are 48 FREF samples representing a symbol. A pseudorandom data sequence is being precalculated in software and it resides in the RAM. During the transmit modulation, the DSP fetches and adds to the FCW (left $y[k]$ feed in Fig. 2) a new sample every six FREF clock cycles, so the actual oversampling ratio is 8, which is quite adequate. The power spectrum of the GMSK-modulated data for GSM is shown in Fig. 18. The GSM mask is met at frequency offsets less than 300 kHz from the carrier. Unfortunately, because in this chip the XIO data cannot be fed into the ADPLL in a two-point

Fig. 17. Observed settling time of the ADPLL.
modulation manner [4], the higher frequency spectrum components get filtered by the single-pole loop attenuation of 8-kHz bandwidth. It would be quite feasible to accurately predistort the input data by preemphasizing the higher frequencies (the ADPLL loop transfer function is almost exact due to its digital nature) in order to extend the flat part of the transfer function, as reported in [12]. However, this task is beyond the scope of this research.

X. CONCLUSION

We have presented implementational details of the first SoC that fully integrates a processor core with a functional RF transmitter for wireless applications. The IC chip is fabricated in a high-density 130-nm digital CMOS process with no analog extensions. The transmitter architecture is based on the ADPLL with a wideband frequency modulation capability, which is built from the ground up using digital techniques that exploit high speed and high density of a deep-submicrometer CMOS process while avoiding its weaker handling of voltage resolution. In this scheme, the 8-b variable phase accumulator counts the number of rising edge transitions of the 2.4 GHz digitally controlled oscillator. To meet the timing that satisfies all of the process, voltage, and temperature corners, the critical path is retimed such that the lower order two bits operate at the full RF rate, while the higher-order six bits operate at RF/4 rate. We have also presented a high-performance flip-flop used in the design of the variable phase accumulator and the TDC. The flip-flop is symmetrical along the vertical axis and provides identical resolution of the rising and falling edge metastability of the input data. The DCO and PA are built as ASIC cells with digital I/Os. The behavior is modeled in VHDL using real-valued signals. The rest of the RF transmitter is synthesizable from RTL subset of VHDL, auto-placed and auto-routed. A portion of the digital logic operates at the 2.4-GHz clock frequency. The use of VHDL allows for a tight and seamless integration of RF with the DSP. Simulation of the entire transmitter is carried out to determine RF performance at the communication packet level. This chip is the first ever to be reported in the literature regarding simulating the complete RF functions in VHDL and co-simulating RF functions with a DSP. The processor is a Texas Instruments TMS320C54x DSP, which is commonly used in cellular phones. The RF transmitter is tightly coupled with the DSP through a parallel bus interface with 16-b data and a dedicated 8-b address space. To demonstrate the tight coupling, a DSP program was written to perform software modulation of the GSM standard. It is the first report of a DSP-driven software modulation of an RF wireless standard in a single-chip environment. The presented IC chip demonstrates feasibility of a cost-effective SoC for software defined radio. The obtained results prove attractiveness and competitiveness of the “digital RF” approach whose goal is to replace RF functions with high-speed digital logic gates.

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REFERENCES

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