The following is derived by looking through the lab documentation and noting locations where:

- it says to do something, e.g., size components, then you need to show how components were sized – not a lot of detail, but enough so TAs realize how you did it.
- a question is asked, you need to answer the question
- an explanation is asked for
- measurement is asked for, you need to show the result, e.g., a neat, well labeled plot, comment on result (TAs don't have time to have to interpret your plot, if the plot shows something, say it, if it doesn't show something, then consider not including it) and of course if you have both theory and measurement, you should compare the two, if they don't agree, explain why (or if you are not sure, mention some likely possibilities). Comparisons are sometimes best done in a table.

Don't include unnecessary extra theory and make sure the text is legible.

Part 1

1. The VCO [12 marks]
   - [2] Choose resistor/cap values for the VCO (basis of choice, any iteration required).
   - [5] Plot of VCO frequency vs. dc tuning voltage.
   - [5] Calculate k_{vco}.

2. The 3 PHASE DETECTORS [17 marks]
   - [6] Plot $v_{average}$ vs phase difference.
   - [6] Compute k_{phase} for each phase detector and compare to theory.
   - [5] Which phase detector is also a frequency detector? Explain.

Part 2

3. The PLL THEORY, transfer function, phase error, sizing components, no marks since this is all covered in Assignment 2.

4. The PLL MEASUREMENTS [29 marks]
   - [5] Plot phase variation vs. input frequency.
   - [5] Explain if lock range is related to ω_n.
   - [5] Plot VCO control voltage vs. signal frequency. Calculate k_{VCO} and compare to earlier measurements.
   - [3] Reduce gain to 1, how did you do this?
   - [6] Calculate new ω_n, ζ.
   - [5] Plot phase variation, v_c compare to previous results with gain = 2, explain similarities, differences, compare lock range.

Part 3

5. The PLL SYNTHESIZER [20 marks]
   - [8] Calculate ω_n and ζ for divide by 3, 4?
   - [4] Are the VCO and reference synchronized? Show waveforms for divide by 3, 4
   - [5] Plot the VCO control voltage while the /N is switching.
   - [5] Explain the plot above. What would the transient look like if it didn't lose lock? Sketch expected waveform.

Other

6. Discretionary Marks [10 marks]
7. Demos Part 1: Oct 25, 26, 27, Part 2: Nov 8, 9, 10 [30 marks]

Total Marks: 118