• **Example:** If $v_{on}$ is picked to be 0.2 V, $V_{DS}$ set to $V_{on} + 0.2V = 0.4V$, $V_{TN} = 0.8V$, $V_{TP} = -0.9V$, power supply rails at 3.0 V, (bias voltages shown below) then swing from about 0.6 V to 2.4 V.

$$\Delta i = g_m v_d/2$$

$\Delta i = 0.2V + 0.4V = 0.8V = 0.9V - \Delta v$  

$0.8V = 0.9V - \Delta v$

• single stage (output current is directly $g_m v_d$) high frequency capability

• $gain = \frac{v_o}{v_d} = g_m R_o$, typical gain about 1000 or 60 dB. $R_o$ is high due to cascodes

• Dominant pole, UGBW is set by load capacitance thus larger load results in more stability

• Set current by desired slew rate and known capacitor load.

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**Common-Mode Feedback Circuits**

• Circuit and feedback often define difference mode

• Common mode can drift, potentially putting circuit into bad region of operation

• Need common-mode correction circuit to provide low $A_c$, with minimal reduction of $A_d$

• Can sum outputs to obtain $v_{oc}$. If this is not zero, feed back a correcting signal. If output is purely differential, $v_{op} = -v_{on}$ and the sum will be zero. An example below uses resistors for summing

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**Example of Common-Mode Feedback Circuit for Folded-Cascode Amplifier**

• Capacitor C across resistor R improves high-frequency performance

• Operation:
  - If both outputs are high, $v_c$ will go high with respect to $v_{ref}$
  - $v_{bias}$ will also go high, since the extra amplifier is non-inverting
  - $M_4$ and $M_5$ will have their current reduced
  - The output voltage will be reduced (overall negative feedback)

• summing: use resistors, switched capacitors, transistors in linear region, or differential pair.

• resistors across output, or SC can reduce DC gain, however, equivalent R can be very high.

• Note: feedback of the appropriate polarity could instead be fed back to $M_3$ or to $M_{10}$ and $M_{11}$.

• Things to watch out for:
  - Stability of CM loop (Tests open loop, or with common-mode step)
  - If summing with SC, restricted to time-domain simulations (or replace with $R_{eq}$)
  - linearity of sum for large diff voltage
Two-stage opamp with pole splitting compensation

Transfer function: \[ \frac{V_o}{V_i} = A_o \frac{\omega p2}{\omega z} \left( s + \frac{R}{R_s R_o} \right) \]

Low Freq. gain: \[ \frac{V_o}{V_i} = \frac{V_o}{V_i} \frac{\omega z}{\omega p2} = A_o = \frac{g_{mo} R_o}{g_{m6}} \]

\( \omega p1 = \frac{1}{R s g_{m6} R_o C} \)

next pole: \[ \omega p2 = \frac{g_{mo}}{C_L} \]

RHP zero: \[ \omega z = \frac{g_{m6}}{C_c} \]

Where: \( v_i = (v_1 - v_2) \), \( g_{mo} = g_{m6} \)

\( g_{m6} = g_{m1} = g_{m2} \), \( R_c = R_o || R_{o5} \), \( R_s = R_{o6} || R_{o7} \)

\( C_z = \text{parasitic (small)}, C_L = \text{load capacitance} \)

- A normal (LHP) zero would add phase lead to improve stability, but RHP zero adds phase lag which reduces stability (45° at \( \omega p1 \)).

- Increased load capacitance reduces stability since \( p_2 \) moves to lower frequency.

- \( p_2 \) and \( z \) must be beyond UGBW enough so total phase shift due to \( p_2 \) and \( z < 45° \).

Rules of thumb: Gregorian and Temes

\( |p_2| = 3 \text{ UGBW} \rightarrow 53° \text{ phase margin} \)

\( |p_2| = 2.2 \text{ UGBW} \rightarrow 60° \text{ phase margin} \)

Small Signal Model

Additions to Pole Splitting, Offsets, Gain Errors, Buffers

The zero in the RHP can result in instability. Can remove, or compensate for with the following techniques:

1. Buffer, typically source follower, to allow feedback only (removing feed forward)

   - This removes the zero, and the system is left with two poles. These should be separated by the DC gain, or more for stability.

2. Series Resistance

   \( v_z \) to \( \omega z = \frac{1}{R_s R \omega z} \), changes \( \omega p3 = \frac{1}{R \omega z} \),

   \( \omega z \rightarrow \infty, \) or bring it into the LHP where it can cancel out \( \omega p2 \) approximately

Offsets

- Output referred \( V_{o, off} \)
- Input referred \( V_{i, off} = \frac{V_{o, off}}{A} \)

Calculation of Gain Error

\[ \frac{V_o}{V_i} = \frac{1/B}{1 + 1/(AB)} = \frac{1}{B} \left( 1 - \frac{1}{AB} \right) \]

Valid for high A.

Here, desired gain = \( \frac{1}{B} \), Gain error \( \frac{1}{AB} \), where \( AB = \text{loop gain} \)

Closed loop gain is \( \frac{1}{B} \) in dB

Buffers

- Source output has low impedance, limited swing, can only get within \( V_T \) from the rails, (assuming \( V_{in} \) can go all the way to the rails).

- Drain output is a current output, i.e., higher impedance compared to source output, but good swing, can get essentially all the way to the rails.
Layout and Cross Sections of CMOS Transistors (Source - Substrate Connected)

schematic

Top view

Cross section

Resistors

\[ R = \rho \frac{L}{A} = \rho \frac{L}{TW} = R_s \cdot \frac{L}{W} \]

- design information documents often give \( R_s \), the sheet resistance in ohms per square. \( R_s = \frac{\rho}{T} \). e.g., if 100Ω/□ then \( R = 100 \times \frac{60\mu}{10\mu} = 600\Omega \) which we see as 6 squares.

- a typical resistor:
  - in counting total length, corner square is about 0.5 square. Result 57 □ →

- Absolute tolerance:
  - \( \pm 20\% \) for wide resistors > 10 \( \mu m \)
  - \( \pm 30\% \) for \( W = 5\mu m \)

- matching: \( W = 5\mu m \pm 3\% \), \( W = 10\mu m \pm 1.2\% \), \( W = 25\mu m \pm 0.8\% \), \( W = 50\mu m \pm 0.2\% \)
Capacitors

- Parallel plates of Area A, capacitance per area \( C_0 \)
  \[ C = C_0 A \quad \text{where} \quad C_0 = \varepsilon_0 \frac{L}{t_{ox}} = \varepsilon_R C_0. \]

- If \( t_{ox} = 0.017 \mu m, \varepsilon_R \) for SiO\(_2\) is 3.9 then
  \[ C_{ox} = 3.9 \times 8.854 \times 10^{-12} \left( \frac{F}{m} \right) = \frac{2 \varepsilon_0 L}{(\mu m)^2} \]
  example:
  \[ 0.017 \times 10^{-6} \left( m^2 \right) \]
  transistor estimate \( C_{gs} = \frac{2}{3} C_{ox} W L \), with \( W = 150 \mu m, L = 1 \mu m \)
  has \( C_{gs} = (2/3) \times 150 \times 2 \left( \text{fF/} \mu \text{m}^2 \right) = 0.2 \text{ pF}. \)

- Capacitors can be metal-metal (MIM), poly-poly or poly-diffusion. (Poly-poly shown below)

- Typically design as multiples of a unit capacitor for best matching, e.g., unit could be 0.5 pF, then could get accurate 1.5 pF match to 2.5 pF.

- Otherwise, need to keep area to perimeter ratio the same.

Transistors

- Often W/L >> 1, so can use multiple contacts for minimal source or drain series resistance

- Diagram same for p or n. If PMOS, then in n-well with p+ mask, NMOS in p-substrate with n+.

- Can have multiple stripes. This can reduce total drain or source area to minimize capacitance.

- Two gate poly stripes, could be common source, e.g., diff pair, or common connection or since we often cannot tell source and drain apart, it might be a series circuit (for Nand, or cascode).

- Can minimize drain area and perimeter of diff pair to minimize capacitance.

- In an opamp, the second (parasitic) pole may be at the drain, so minimum capacitance here can help to increase freq response.

- Can interleave two transistors, as in the example above, where there are a total of eight transistors of which four form M1 and four form M2.

- This minimizes the effect of process variations and temperature variations across the chip, thus resulting in better matching, and lower offset. This is called the common-centroid topology.

- Note: the same interleaving technique can be used for two resistors which need to be matched.