Carleton University - Fall Term 2020-2021 - ELEC-5401

Signal Integrity in High-Speed Designs

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Course Objectives and Overview

1) To understand signal integrity issues in high-speed designs
2) To become knowledgeable of signal integrity and interconnect design/modeling/simulation methodologies

The rapid growth in VLSI circuit technology coupled with the trend towards complex/miniature devices is placing enormous demands on computer-aided design (CAD) tools focused on microelectronics. The design requirements are becoming very stringent, demanding higher operating speeds, sharper excitations, denser layouts and low power consumption. Consequently, signal integrity issues such as delay, attenuation, crosstalk, ground bounce etc. are becoming major bottlenecks in design and validation of high-speed circuits and systems.

High-speed effects, if not addressed properly during the design stage, can cause logic glitches which render a fabricated digital circuit inoperable, or they can distort an analog signal such that it fails to meet specifications. Since extra iterations in the VLSI design cycle are extremely costly, accurate prediction of these effects is a necessity in high-speed designs. A paradigm shift is currently taking place in both the design and CAD community to adapt to the new requirements of high-speed design issues. However, currently available CAD tools and design strategies do not handle the complex scenario of high-speed circuit design/analysis encompassing diverse domains, adequately.

This course would focus on understanding signal integrity issues, developing new generation CAD tools to model and simulate these effects, and also on developing design strategies to handle them. Following is a broad outline of the materials proposed to be covered in this course:

- Brief Review of Computer-aided Design for Circuit Analysis, Modified Nodal Analysis, Frequency Domain Analysis, Transient Analysis
- High-Speed Design and Signal Integrity Issues, Industry need/directions, signalling in design hierarchy: Chip, Package, PCB; Signal Integrity Practitioner's View.
- Signal Parameters, Frequency-time relations. Clocking Schemes and Clock Components, Latches. Synchronous Systems. Issues: Clocking Skew, Jitter, Inter Symbol Interference, Rise/Fall Time Degradation. Eye Diagrams, BER and other SI Analysis Metrics and Tools.
- Interconnect Parameters: Resistance, Capacitance, Inductance and Conductance. Related Concepts and parameter extraction.
- Modeling of High-speed Interconnects/Packages: Elmore Delay, RC Trees, Lumped Models, T, Pi Structures, Coupled, Lossless and Lossy Lines
- Distributed Interconnects: Telegraphers Equations, SPICE compatible frequency-domain stamps, mixed frequency/time analysis issues.

- Macromodeling: Method of Characteristics, Macromodeling Issues: Accuracy, Stability, Passivity, and Causality. Matrix Rational Approximation (MRA) based macromodels.
- Current Distribution Related Effects: Skin, Proximity and Edge Effects, Frequency-Dependent RLGC parameters, Non-uniform Transmission lines, Full-wave models.
- Differential Transmission Lines. IBIS: Behavioral Models. Electromagnetic Compatibility and Interference issues.
- Power Integrity: Power Distribution Issues and Systems, Target Impedance, Ground Bounce Analysis, Packaging Structures. Theory of Decoupling Capacitors.
- Measurements: TDRs and VNAs, Multiport parameters, Concept and Underlying Theory of Scattering Parameters, Errors in the Data, Rational Function Based Macromodels, Vector-fit, SPICE compatible Realizations.
- System Architecture improvements for High-speed Channel Design, Serdes, Differential Signaling.
- Concurrent Mixed-domain Analysis: Circuit, EM, MEMS and Optical Devices., Managing complexity via model order reduction, High-Speed Design Strategies.

Books (recommended reading)

E. Bogatin, *Signal Integrity Simplified*, NJ: Prentice-Hall, 2004.

H. B. Bakoglu, Circuits, *Interconnections and packaging for VLSI*, MA: Addison-Wesley, 1990.

D. Brooks, *Signal Integrity Issues and Printed Circuit Board Design*, NJ: Prentice-Hall, 2003.

S. Hall, G. Hall, and J. McCall, High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices, Wiley-Interscience, 2000.

B. Young, *Digital Signal Integrity: Modeling and Simulation with Interconnect Packages*, NJ: Prentice-Hall, 2001.

M. Swaminathan and A. E. Engin, *Power Integrity Modeling and Design for Semiconductors and Systems*, NJ: Prentice-Hall, 2007.

C. Paul, *Analysis of Multiconductor Transmission Lines*, NY: John Wiley and Sons Inc., 1994.

H. W. Johnson and M. Graham, *High-speed Digital Design*, NJ: Prentice-Hall, 1993.

R. K. Poon, *Computer Circuits Electrical Design*, NJ: Prentice-Hall, 1995.

R. Achar and M. Nakhla, "Simulation of High-Speed Interconnects", *Proceedings of The IEEE*, Vol. 89, pp. 693-728, May 2001.

Also, additional hand-outs will be recommended in the class.

Prerequisites

Familiarity with the basic concepts in circuit theory/design, linear algebra and calculus.
Lecture Delivery: Online (using Carleton's integrated BBB and CuLearn Platform)

Grading

Assignments (2)	40%
Final Exam	60%

Office Hours (3036 MC): Wed – 4:00 - 5:00 pm.

Course Web-site: Elec5401 link in CUlearn