ELEC 4609 Integrated Circuit Design and Fabrication

Instructor: Prof. Rony E. Amaya

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Lectures: Tue, Thu 10:05 -11:25 ONLINE

Office Hours: By Appointment - ONLINE

TAs:

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Office Hours: **By Appointment - ONLINE**

The Course outline can be accessed through the 'Syllabus' page, below.

Marking Scheme

Final exam 25% (The final exam is for evaluation only and will not be returned)

CUSOI IC design project: 30%

CMOS IC OpAmp Project: 30%

Assignments and Quizzes: 15%

IC Design Project

The most important component of ELEC4609 is the IC design composed of two parts: 1) Design, Fabrication, and testing of a CMOS integrated circuit at Carleton University (CUSOI) and 2) Layout and verification of an Operational Amplifier based circuit that could include a bandgap reference circuit, a voltage regulator or a switched capacitor filter. For part 1) We will attempt to fabricate the circuits here at Carleton and return finished silicon chips for testing before the end of the term. For part 2) students will use a state-of-the-art CMOS process and design and verify an operational amplifier meeting required specifications. Students are encouraged to work in pairs on part 1), and submit a single report. Each member of the team must understand all aspects of the design and clearly identify his/her contributions to the report. In order to allow time for chip fabrication, there will be tight deadlines for the design submission. Project sign-up should be completed by September 13. A complete schematic verified by SPICE simulation is due on September 27. A fully verified layout implementing the schematic ready for fabrication is due on October 16. This layout must be submitted at this time to obtain credit for the course. A comprehensive report on the project will be due towards the end of the term. For part 2) students will work individually and design report will be due on the last day of classes.

Assignments and Labs

The IC design and Op-Amp project sections require many hours of work with CAD tools, and inevitably much of this work will be done outside scheduled lab periods. Due to COVID-19 restriction, all labs will be delivered online. TAs will provide technical assistance remotely as well as provide live demos. The formally scheduled lab periods provide an opportunity to have a TA review and comment on your work remotely. Lab 1 will provide a tutorial introduction to the CAD tools we will use. In addition to the term IC design project, there will be several assignments on the fundamentals of CMOS process design. Formal labs begin Sep. 12 but you are strongly encouraged to start working on Lab 1 on your own before that date. For access to Cadence and/or technical tool issues contact scott.bruce@carleton.ca.

Topics:

1. Circuits and Layout

Basic CMOS structure and process flow. The relationship between layout and cross-section. Design rules. Introduction to CAD tools for schematic capture, circuit simulation (SPICE) and layout. CMOS inverter: transfer characteristic, ratioing, noise margin, rise and fall times. Advantages of CMOS. NAND and NOR gates. Transmission gates. Dynamic logic. Input protection. Driving large capacitive loads with output buffers. Latch-up. Introduction to analog CMOS circuits: differential amplifiers, source follower buffers, current mirrors, device matching, temperature compensation.

2. Op-Amp Circuit Design, Layout and Verification

Fundamentals of Op-Amp design, current mirrors, input differential pair, output stages. Gain and stability including pole-splitting. Advance analysis including PSRR, phase margin and more. Analog Circuit Layout fundamentals including matching, symmetry, common-centroid, and others. Full Analog verification including post-layout extraction, Analysis under PVT variations. DRC. LVS verification using commercial software. Op-Amp based circuits will include Bandgap references, LDO regulators, and Switched-Cap filters.

3. CMOS Process Technology

Overview of the processes required to fabricate a MOS IC: oxidation, ion implantation, diffusion, thin film deposition, photolithography, and etching. Integration of basic steps into a simple CMOS process flow. Short channel effects, hot carrier effects, and techniques for suppression. Evolution of CMOS technology: shallow trench isolation, high-k dielectrics, strained silicon... The future of microelectronics.

Recommended (but not compulsory) textbook:

R. Jacob Baker, Harry W. Li, and David E. Boyce, CMOS: Circuit Design, Layout, and Simulation, 3rd ed, 2010 IEEE Press, ISBN 0-7803-3416-7 (can be ordered online through IEEE or Chapters)

Alan Hastings: The Art of Analog Layout, 1st ed, 2000. ISBN-10:0130870617 (can be ordered online through IEEE or Chapters)

Health and Safety

See http://www.doe.carleton.ca/undergrads/health-and-safety.pdf for general Health and Safety: See http://www.doe.carleton.ca/undergrads/health-and-safety.pdf for general guidelines. Normal precautions in working with low-voltage electrical equipment must be taken when testing projects. Students volunteering to assist in multi-project chip fabrication in the Carleton Microfab must complete special training and must be WHMIS qualified.

Plagiarism

Plagiarism is a serious instructional offense that will not be tolerated. It involves passing off someone else's original work as your own. Most cases of plagiarism can be avoided by carefully citing sources for any ideas, statements, results etc. that are not your own. Please refer to the section on instructional offenses in the Undergraduate Calendar for additional information.

Academic Accommodation

You may need special arrangements to meet your academic obligations during the term. For an accommodation request the processes are as follows:

Pregnancy obligation**:** write to me with any requests for academic accommodation during the first two weeks of class, or as soon as possible after the need for accommodation is known to exist. For more details visit the Equity Services website:
http://carleton.ca/equity/accommodation/student_guide.htm

Religious obligation**:** write to me with any requests for academic accommodation during the first two weeks of class, or as soon as possible after the need for accommodation is known to exist. For more details visit the Equity Services website: http://carleton.ca/equity/accommodation/student_guide.htm

Students with disabilities requiring academic accommodations**:** in this course must register with the Paul Menton Centre for Students with Disabilities (PMC) for a formal evaluation of disability-related needs. Documented disabilities could include but are not limited to mobility/physical impairments, specific Learning Disabilities (LD), psychiatric/psychological disabilities, sensory disabilities, Attention Deficit Hyperactivity Disorder (ADHD), and chronic medical conditions. Registered PMC students are required to contact the PMC, 613-520-6608, every term to ensure that I receive your *Letter of Accommodation*, no later than two weeks before the first assignment is due or the first-in-class test/midterm requiring accommodations. If you only require accommodations for your formally scheduled exam(s) in this course, please submit your request for accommodations to PMC by the last official day to withdraw from classes in each term. For more details visit the PMC website:
http://www.carleton.ca/pmc/students/acad_accom.html