ELEC 4706 Digital Integrated Electronics - Winter 2019

Instructor: Prof. Rony E. Amaya
email: rony.amaya@carleton.ca
Lectures: Wed, Fri 11:35-12:55 in ME 4342
Office Hours: Tue 10:00-11:30 in ME 5144

Objective:

This course builds upon the digital and analog design knowledge acquired in preceding courses.

The course addresses the major design challenges faced by digital designers today. New interfacing techniques based on high-speed serial data links are introduced. Modern memory devices are overviewed. Examples of memory and CPU interfacing are given.

The HDL simulation is a major part of the design process. Fundamentals of the HDL, event-driven simulator operation are discussed. Programmable Logic Devices are presented as an extension of a standard digital ICs design technique. Evolution into FPGA and relation to Standard Cell and Structured IC design is presented.

Operation at higher speed (digital chip up to 1GHz clock and mixed-signal digital chips up to 40GHz clock) changes design practices. Factors influencing these new designs would e discussed. The design of digital integrated circuits has evolved into a fully automated process that starts with a behavioral or structural description of the circuit and uses synthesis as a link to a given implementation technology.

The highest speed digital design does not follow this route, it uses transistor level design. It is called "mixed-signal" design and includes transceiver blocks that process digital data transmitted over interconnect channels. The transmission is lately performed by a serial interconnect where single bit (or symbol) is send/received at a time. The concepts behind serial data transmission (data rate, BER, eye-diagram, jitter, jitter tolerance etc.) as well as examples of transmitter, channel and receiver devices will be provided.

TA and office Hours:

TA Name	e-mail	Office Hours / Location
Jacob Pike	jacobpike@cmail.carleton.ca	Thursday 11:30-12:30 / AP338*
Soroush Sheikhpour	soroushsheikhpourkou@cmail.carleton.ca	Monday 5:30-6:30 / CB3303*

*Office hours will be held in the actual lab

Lecture Outline (3 hours per week)

The topics covered are:

1. Review of the laboratory hardware;
2. Circuit, structural and behavioral representation; Elements of VHDL modeling; Digital, event-driven simulator operation
3. Structures of the PLD devices; FPGA vs. Gate Array and Standard Cell design
4. Design Flow; verification
5. Timing; DLL in Digital Design
6. Review of modern memory devices
7. Interfacing a microprocessor to a memory – classical bus design
8. High-Speed serial data links. Signal integrity issues - definition of terms; Signal integrity time domain and frequency domain analysis
9. Serial data transmission receiver/transmitter design

Laboratory (3 hours, every week)

The major component of the course is the laboratory. Please refer to the Lab Manual and additional material for instructions and guidelines. Note labs are to be completed in groups of two and one report is due one week after your scheduled session on CuLearn by 11:30 pm. The penalty for late submissions is = 5 + e^x , where x = number of days late. Also note that you must submit a report for all labs in order to pass the course. Note that labs begin on Monday Jan 14, 2019.

Lab schedule:

Group A1: Monday 14:35 - 17:25, Rm 4135 ME
Group A2: Thursday 8:35 - 11:25, Rm 4135 ME

Assignments

Assignments will be given for this course but not marked. Answers will be posted by the end of the term.

Midterms

There will be ONE midterm for this course during lecture hours (11:35 am to 12:55 am).

Midterm #1: Wednesday, March 20 in ME4342.

Grading:

- Laboratory 30%
- Assignments 10%
- Midterm 20%
- Final Exam 40%

- All labs. assignments and midterms must be completed with an average grade of 50% or better to pass the course. At least 50% on the final exam is required to pass the course.
- As per standard practice in the Faculty of Engineering, students will not be allowed to see their final exams.
- Academic accommodation for any reason must be sought as soon as possible, preferably early in the term. Verification will be required.

Textbook:

1. ELEC 4706 Course Notes and Lab Manual (Main source and available on web)
2. William Dally, Digital Systems Engineering - Cambridge Publishing - ISBN-13: 978-0521061759 - ISBN-10: 052106175X (Strong reference)

References:

1. Charles Roth, **Digital Systems Design using VHD**L , Thompson Engineering - **ISBN-10:** 0534384625 - **ISBN-13:** 978-0534384623
2. Michael D. Ciletti; **Modelling and Synthesis and Rapid Prototypying with te Verilog HDL**; Prentice Hall, 1999
3. Janick Bergeron; **Writing Testbenches – Functional verification of HDL model**s; Springer 2003

4. Steven Brown, Zvonko Vrasenic; **Digital Logic with VHDL Design**; McGrawHill 2009
5. J. Bashker; **A VHDL Primer**; Prentice Hall; 1995
6. Geoff Lawday et al.; **A signal Integrity Engineer's Companio**n; Prentice Hall 2008
7. Eric Bogatin; **Signal and Power Integrity**; Prentice Hall 2010
8. Sudhar Yalamanchili; **VHDL Starter's Guide**; Prentice Hall 1998
9. Kenneth L. Short; **VHDL for beginners**; Prentice Hall 2009
10. VHDL web resources:

- VHDL Reference Guide From Xilinx -- http://www.scribd.com/doc/7307470/VHDL-Reference-Guide-From-Xilinx
- For quick check reference -- http://www.vhdl-online.de/ref93
- There is also a brief relevant tutorial -- http://www.vhdl-online.de/tutorial/englisch/inhalt.htm

Student Responsibilities in the Laboratory

1) Attend each lab punctually. Absence (without permission of the instructor) means NO MARK for that lab. If you have a valid reason for missing a scheduled lab, the lab must be completed as soon as possible after the scheduled lab period.
2) Be prepared for the lab experiment by reading the lab instruction sheets before entering the lab. You will be part of a lab group, but each student must submit his/her own lab report. The lab report is due one week following the scheduled lab period.
3) NO FOOD or DRINK is permitted in the lab or computer rooms.
4) Before entering the first lab, read the Health and Safety Issues in the Microwave Labs document.

Academic Accommodation

You may need special arrangements to meet your academic obligations during the term. For an accommodation request the processes are as follows:
Pregnancy obligation: write to me with any requests for academic accommodation during the first two weeks of class, or as soon as possible after the need for accommodation is known to exist. For more details visit the Equity Services website: http://carleton.ca/equity/accommodation/student_guide.htm
Religious obligation: write to me with any requests for academic accommodation during the first two weeks of class, or as soon as possible after the need for accommodation is known to exist. For more details visit the Equity Services website: http://carleton.ca/equity/accommodation/student_guide.htm
Students with disabilities requiring academic accommodations: in this course must register with the Paul Menton Centre for Students with Disabilities (PMC) for a formal evaluation of disability-related needs. Documented disabilities could include but are not limited to mobility/physical impairments, specific Learning Disabilities (LD), psychiatric/psychological disabilities, sensory disabilities, Attention Deficit Hyperactivity Disorder (ADHD), and chronic medical conditions. Registered PMC students are required to contact the PMC, 613-520-6608, every term to ensure that I receive your Letter of Accommodation, no

later than two weeks before the first assignment is due or the first in-class test/midterm requiring accommodations. If you only require accommodations for your formally scheduled exam(s) in this course, please submit your request for accommodations to PMC by the last official day to withdraw from classes in each term. For more details visit the PMC website:
http://www.carleton.ca/pmc/students/acad_accom.html
Health and Safety Issues All students and TA's are required to read the Health and Safety Document at www.doe.carleton.ca/Courses/ELEC4503/health-and-safety.pdf .

In case of emergency call 613-520-4444 or just 4444 on Carleton Phones.