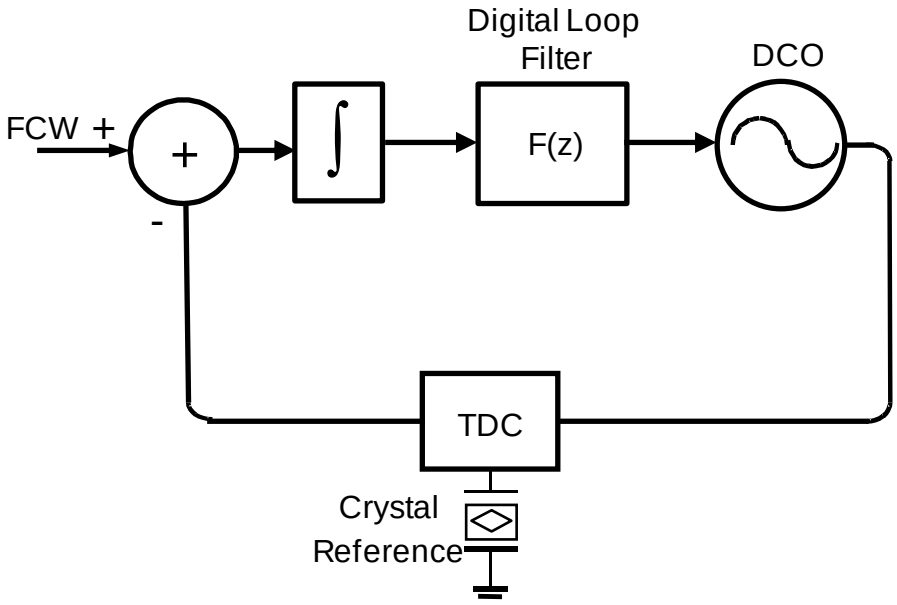
ELEC 5705 RF System Design: Assignment #3

Due April 24th, 2012

The goal of this course will be to come up with a complete architecture for a radio. This third assignment will be to specify the block diagram and specifications for the synthesizer. Reports will be in the form of a 15 page report. For this assignment you must design an ADPLL to generate the LO in your radio.

For the assignment you should build a loop as follows:



You should build all components out of behavioral blocks (as a suggestion use Simulink).

1) To start demonstrate a loop with a loop bandwidth to 150kHz, $\zeta = 0.707$, $F_{ref} = 40MHz$ and $F_{DCO} = 4GHz$.
2) Use a simple integer TDC in this loop.
3) Determine the spur levels at the output of the DCO when the loop is settled for a non-integer division ratio of your choice.
4) Now simulate the loop for parameters that fit your radio design.
5) How much would the spur performance have to be improved to meet your specifications?