ELEC3509 – Lab 1 – Marking Scheme

The marks are generally weighted as follows:

- 50% for showing how you obtained your results
- 50% for explaining what your results mean

Prelab

The prelab is worth **5 marks** and must be completed for **Day 1**.

To receive prelab marks, you must present the following:

- Part 2:
  - Values for R_1, R_B and R_C and how you selected them
- Part 3:
  - Exact equation for I_{out} of current mirror
  - Simplified equation for I_{out} of current mirror
  - Values for R_{E1}, R_{ref} and maximum R_L for 1:1 and 1:4 current mirror/multiplier
  - Labelled schematic for PNP current mirror

Checkout

The checkout is worth **5 marks** and must be completed for **Day 2**.

To receive checkout marks, you must present the following:

- All Parts:
  - Component Tables (Name, Design Value / Measured Value)
  - Data Tables (Name, Design Value / Measured Value)
- Part 2:
  - I_C – V_{CE} plot
  - V_{BE} – V_{CE} plot
- Part 3:
  - Table of Components (Name, Design Value, Measured Value)
  - I_{out} – R_L plots (1:1, 1:4, PNP)
  - V_{out} – I_{out} plot
- Part 4:
  - Current gain – frequency plot

Report Marking Scheme

This table provides the minimum requirements and the total available marks for each. Completing only the minimum requirements is NOT sufficient to receive full marks.

Section	Min. Requirements	Available Marks
Introduction		5
Transistor DC Characterization		
	Prelab: Design Calculations for DC Bias Network	8
	Part 1 – Terminal Voltages	2
	Part 2 – I_C-V_{CE} Plot	6
	Part 2 – V_{BE}-V_{CE} Plot	4
Current Mirror Design		
	Prelab: Design Calculations for Current Mirrors	8
	Part 3 – I_{out}-R_L Plots	8
	Part 3 – V_{out}-I_{out} Plot / Output Impedance	6
Transistor AC Characterization		
	Part 4 – h_{ie}/h_{fe} Calculations	4
	Part 4 – Current Gain-Frequency Plot	8
	Part 4 – Hybrid π-Model Calculations	6
Conclusion		5
Overall Writing and Organization		20
	TOTAL	90